Boolean Algebra – Set 2

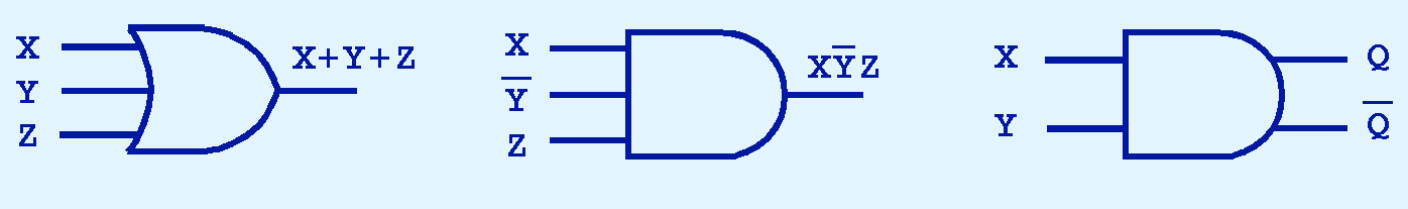
Appendix C (on the text DVD)

C.1,2,3,5,6,7,8,9

Also – Computer Organization & Architecture – Null & Lobor notes

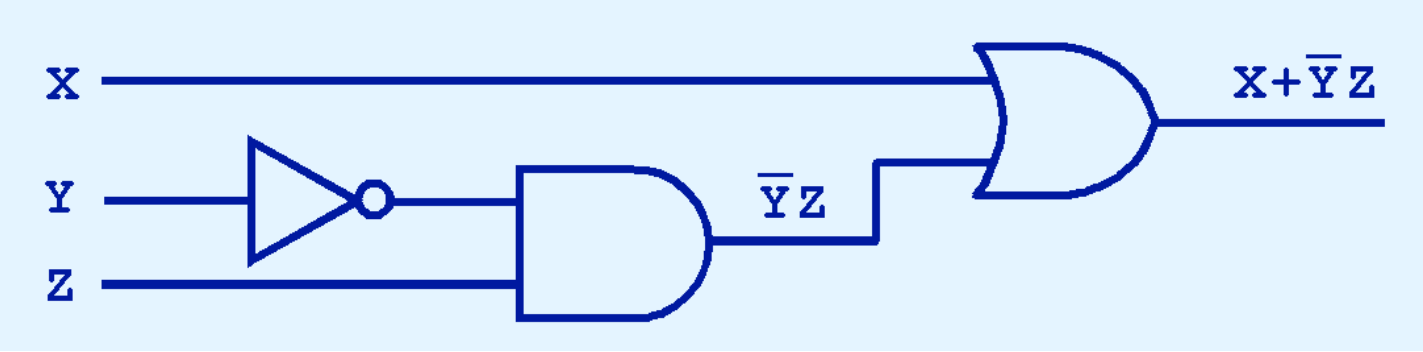
Logic Gates

- While most of what we have dealt with have been two-input gates (one input always for the NOT) you can have more inputs and even more than one output
- Fan-in => number of input allowed
- Fan-out => number of outputs allowed



Multi-Level Logic Circuits

- The number of levels in a circuit is the maximum number of gates from input to output. The following is a 3-level circuit.



Combinational Logic Circuit (CLC)

- A combinational Logic Circuit accepts a binary input and produces a binary output as a function of (only) that input.

Combinational Logic Circuit (CLC)

- An example of a CLC is a parity checker
  - The input is 3 bits and the output is a 1 if the number of 1's in the input is odd, and a 0 if the number of 1's in the input is even

X Y Z	F(X,Y,Z)
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	0
1 0 0	1
1 0 1	0
1 1 0	0
1 1 1	1

CLC

- Another example of a CLC is a half-adder

Inputs		Outputs	
X	Y	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

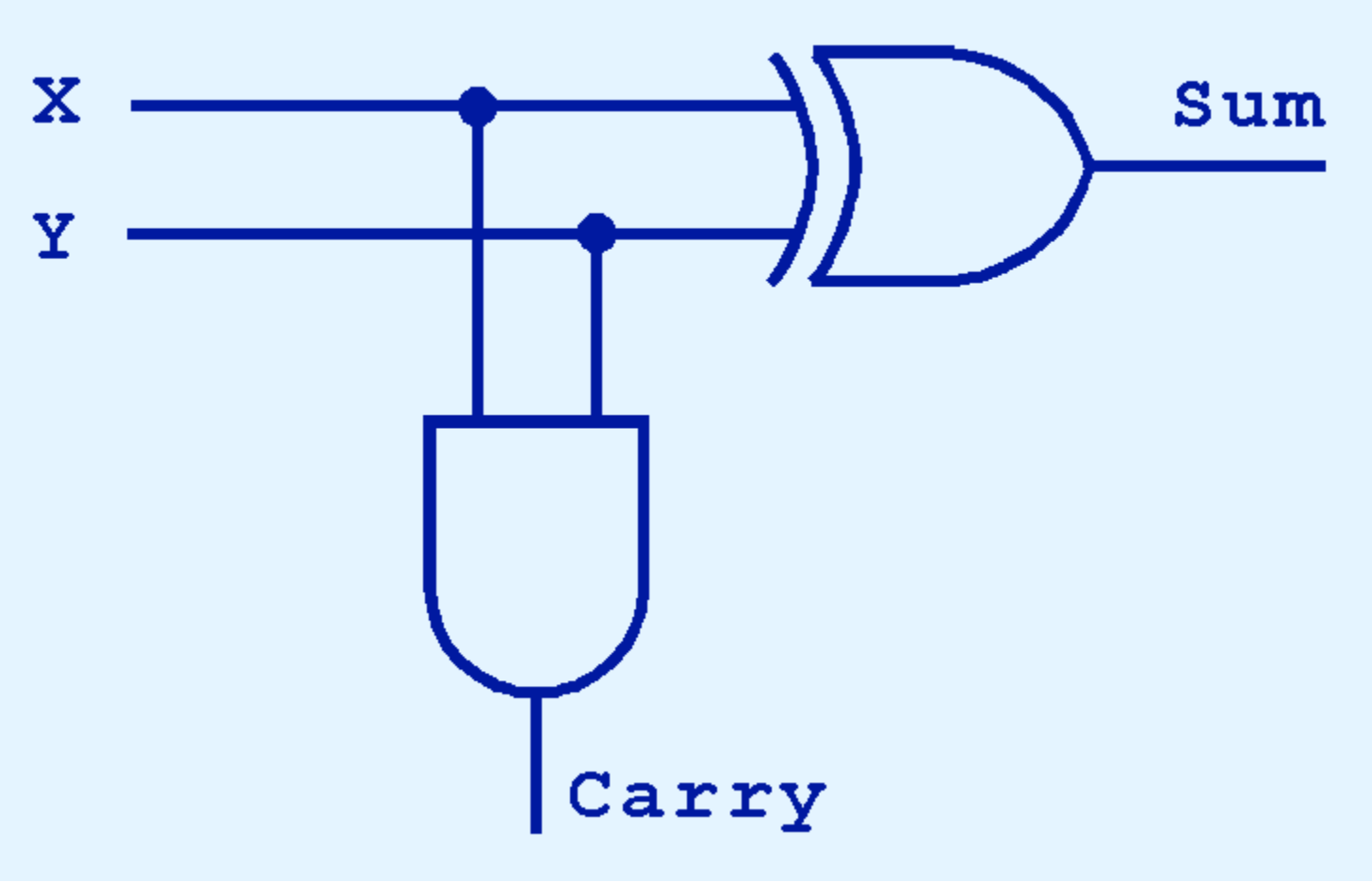
CLC

- Notice that this function is really two functions and so there are really two circuits to implement. As a SOP these functions are:

  sum(x,y) = x'y + xy' = x XOR y

  carry(x,y) = xy

CLC – Half Adder Circuit



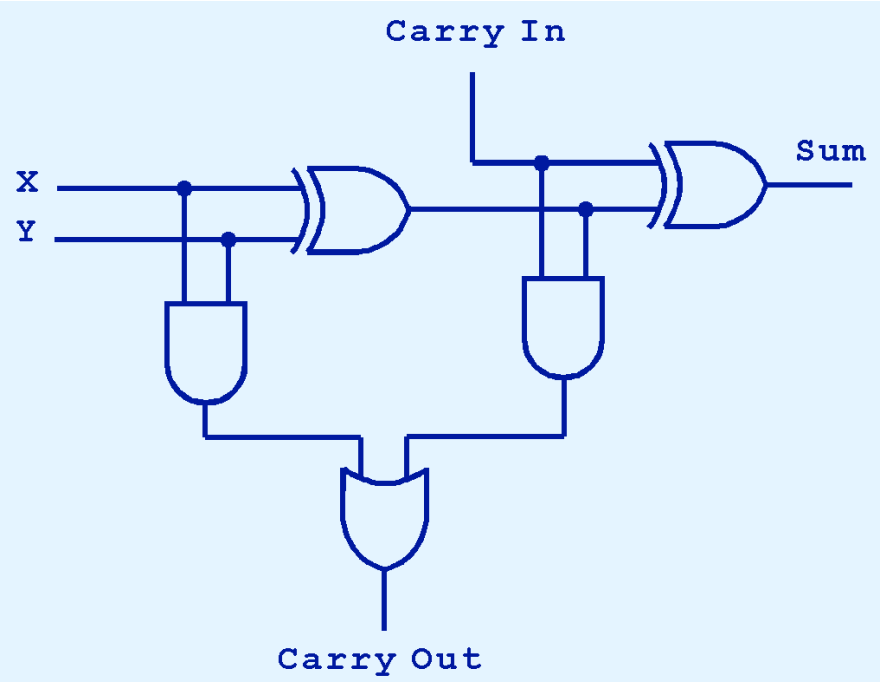
CLS Full Adder

- A full adder differs from a half adder in that its input is the two bits of the numbers being added, and the carry out from the preceding bits' sum.
- Thus, the full adder is needed for summing all bits except the least significant bits.

CLS Full Adder

Inputs			Outputs	
X	Y	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

CLS Full Adder



Inputs			Outputs	
X	Y	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

CLC Full Adder

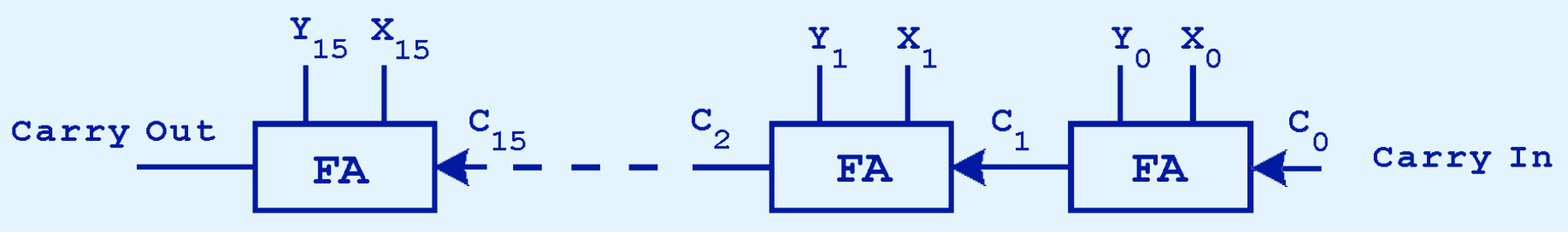
- Notice that in the previous slide the circuit was not set up as SOP or POS
- What would have been different if we had used SOP or POS?
- How many levels are there in the previous circuit?

CLC Full Adder - Question

- Let's say that every gate in the full adder circuit has a propagation delay (the time between the input changing and the output changing to reflect the changed input) of 5 ns.
  - What is the maximum rate at which the circuit can perform an add?
- If we had a 32-bit adder made up of these full-adders, how fast could it perform such adds?

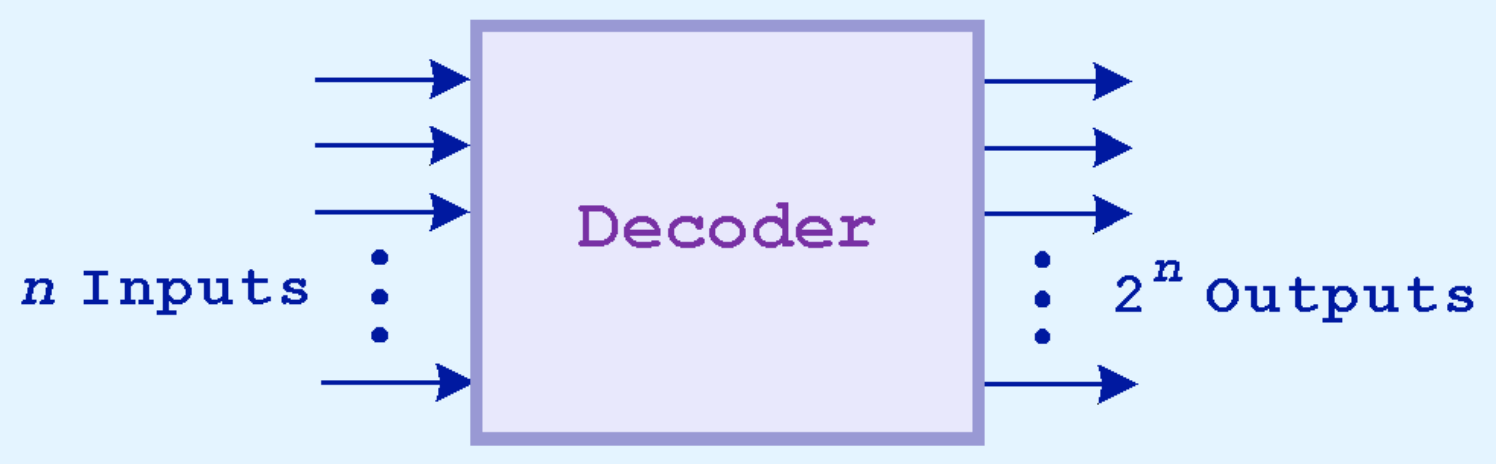
Full Adder – Ripple Carry

- One can combine individual full adders to form an n-bit adder.
- Such a design is called a ripple-carry adder.



Decoders

- There are many other types of circuits that are classified as medium scale integrated circuits. One such device is a decoder.
- A decoder accepts an n-bit input and produces 2^n outputs, only one of which has a value of 1

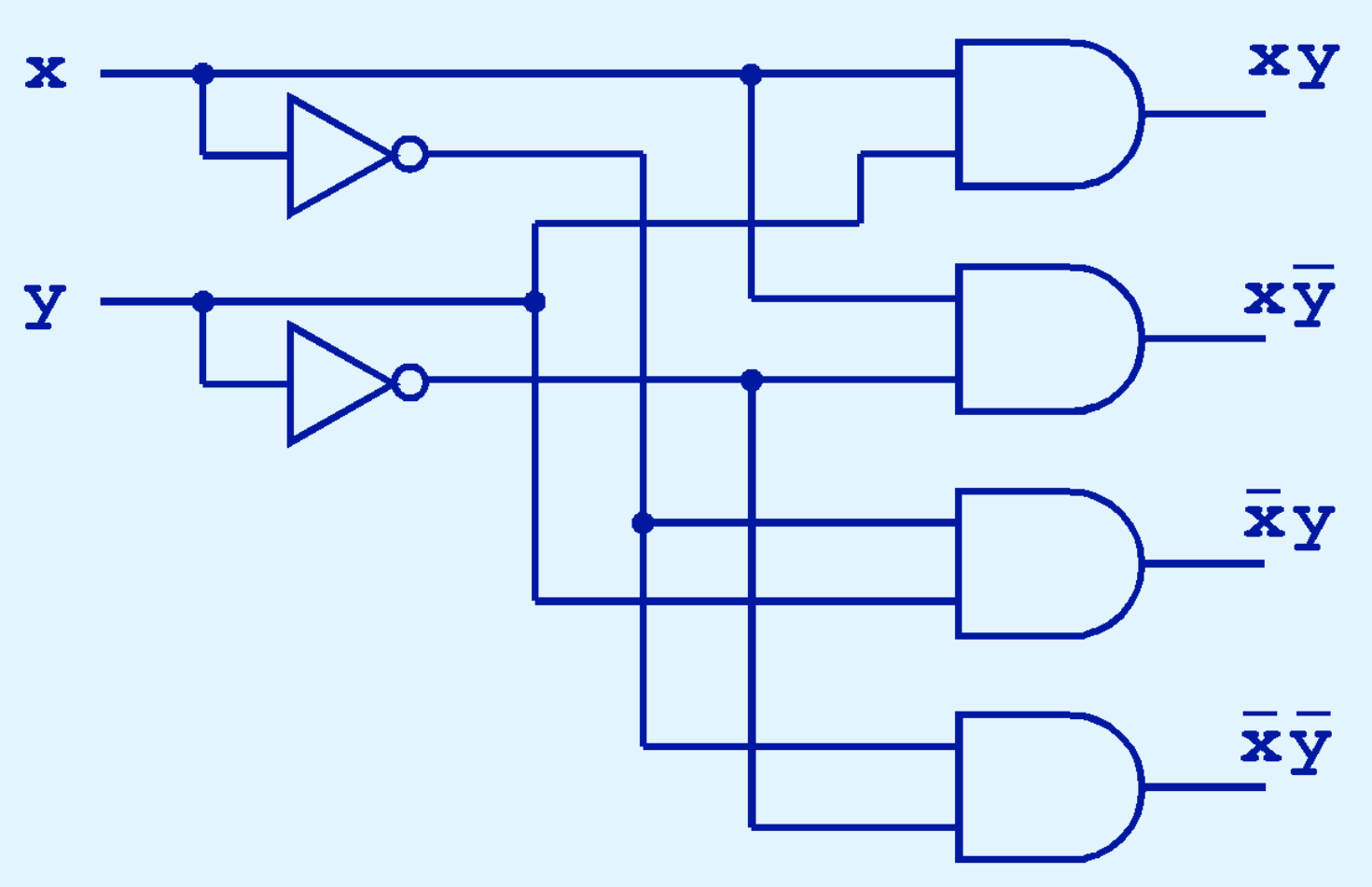


Decoder

- Decoders are used to select a memory location for a read or a write

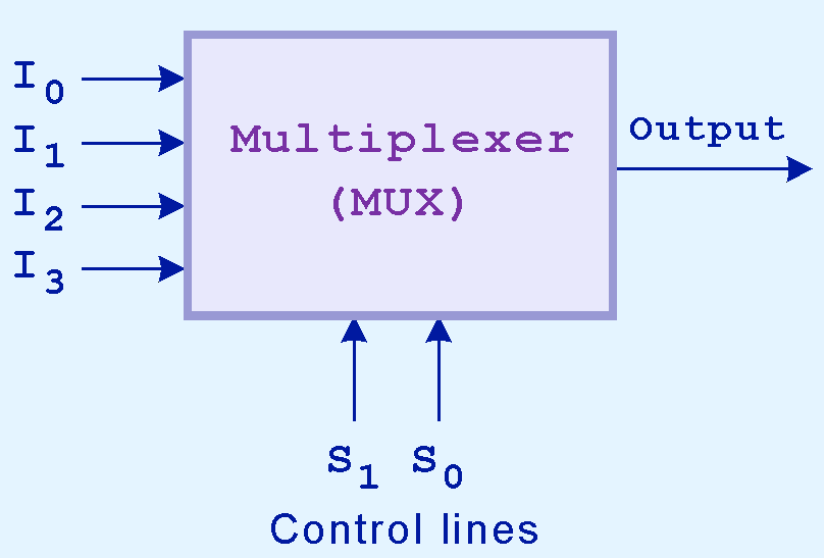
- Develop the truth table and Boolean expression for a 2-to-4 decoder

Decoder

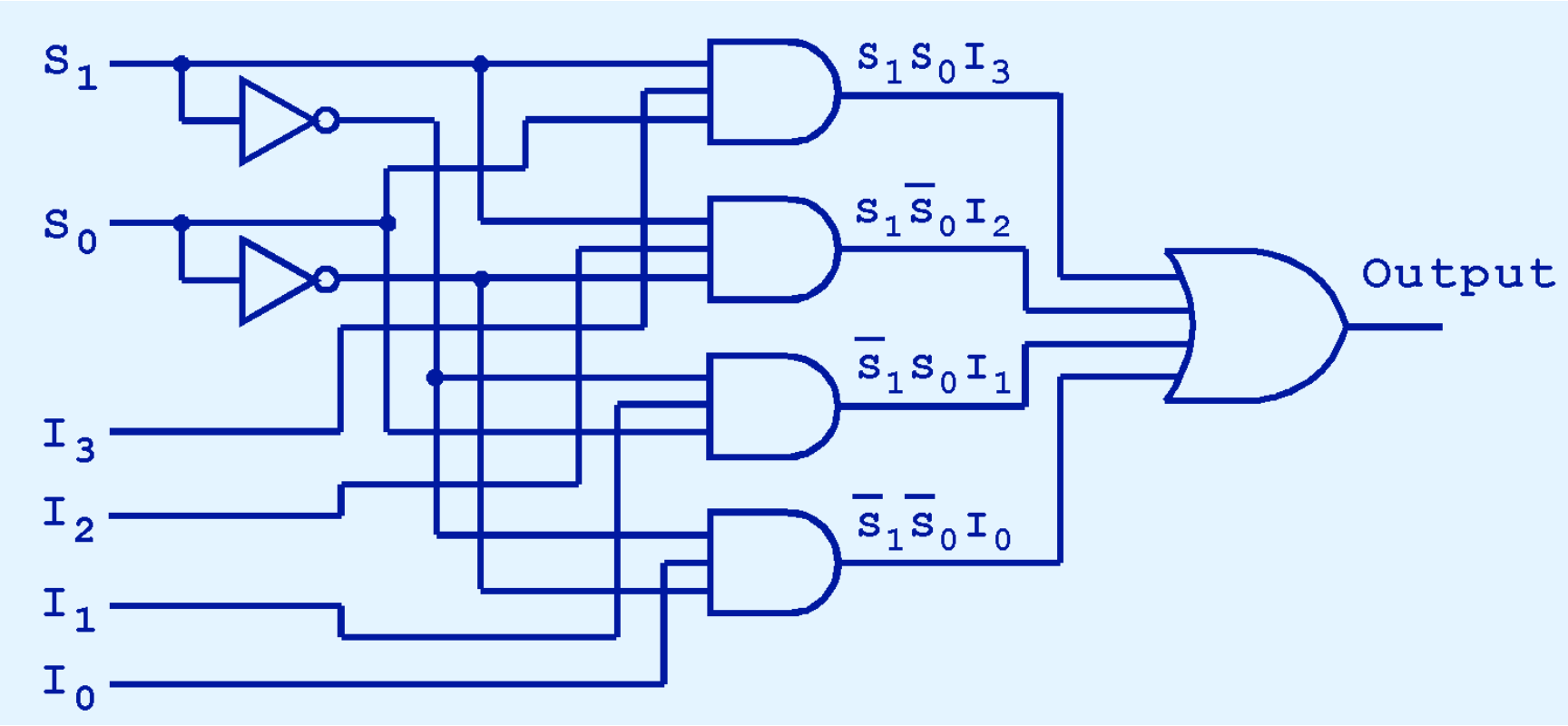


Multiplexer

- A multiplexer does sort of the opposite of a decoder
- Has n inputs and log (n) control lines. Those control lines select one of the n inputs as the output



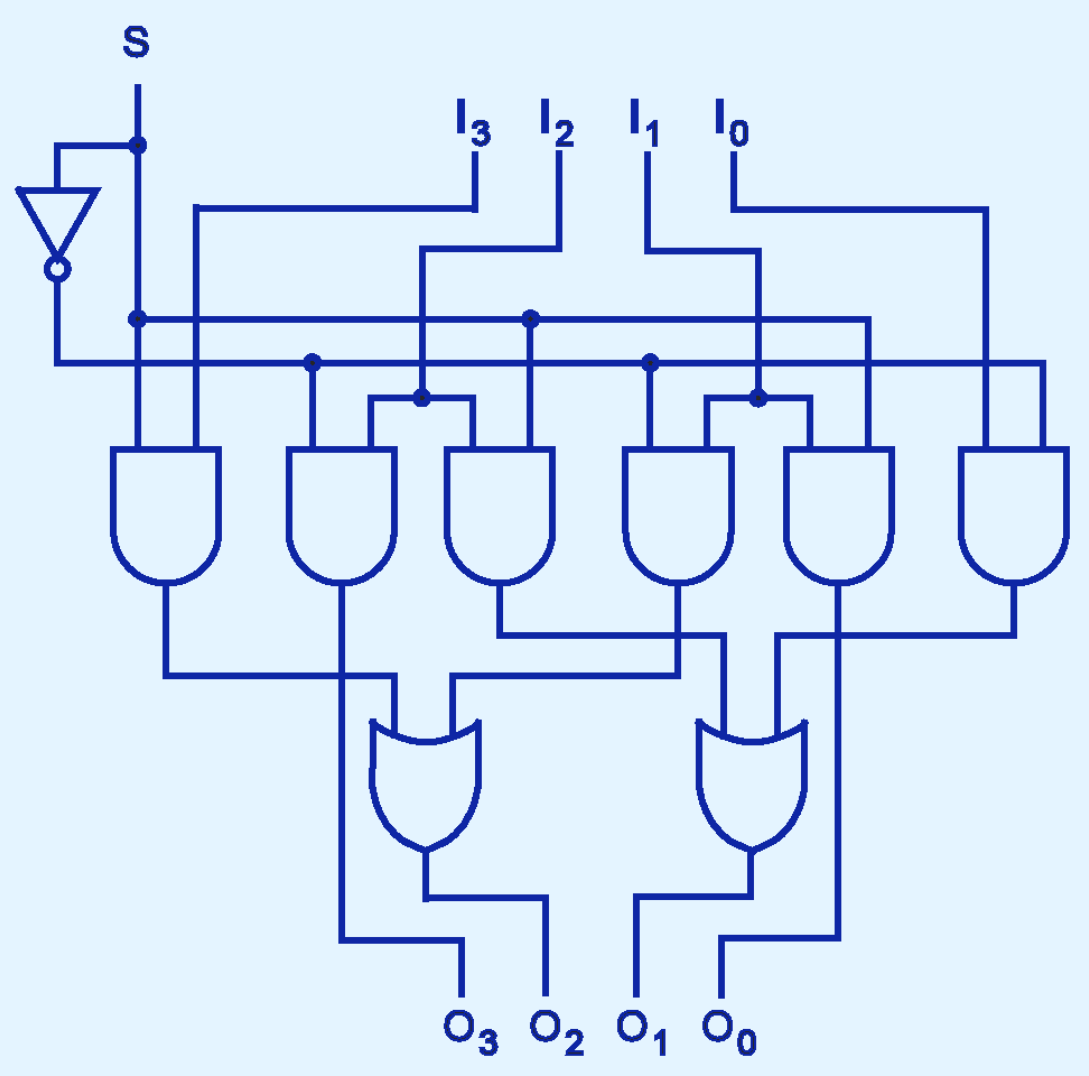
4-to-1 Mux


S_1
S_0
I_3
I_2
I_1
I_0
$S_1 S_0 I_3$
$S_1 \overline{S}_0 I_2$
$\overline{S}_1 S_0 I_1$
$\overline{S}_1 \overline{S}_0 I_0$
Output

Multiplexer

- What is the software equivalent of a multiplexer?

What is this?



Shifter

- The preceding was a shift register.
- If S=0 which way does it shift?